WHAT IS CLAIMED IS:

1. An on-chip real time clock module for use on a digital processing integrated circuit, the on-chip real time clock module comprises:

a plurality of persistent registers to store operational parameters and timing parameters of the digital processing integrated circuit, wherein the plurality of persistent registers are power by a battery and receive a timing signal from a crystal oscillator;

a clock domain crossing module operably coupled to the plurality of persistent registers, wherein the clock crossing domain module synchronizes a crystal oscillator clock domain produced by the crystal oscillator and a system clock domain produced by a system clock circuit of the digital processing integrated circuit;

an input buffer operably coupled to receive operational parameters and timing parameters from the digital processing integrated circuit in accordance with the system clock domain and to provide the operational parameters and timing parameters to one of the plurality of persistent registers in accordance with the crystal oscillator clock domain; and

an output buffer operably coupled to retrieve operational parameters and timing parameters from the plurality of persistent registers in accordance with the crystal clock domain and to provide the retrieved operational parameters and timing parameters to the digital processing integrated circuit in accordance with the system clock domain.

2. The on-chip real time clock module of Claim 1 that further comprises an interface between the on-chip real time clock module and the digital processing integrated circuit.

3. The on-chip real time clock module of Claim 1, that further comprises a controller operable to direct the on-chip real time clock module to store operational parameters and timing parameters from the digital processing integrated circuit or retrieve operational parameters and timing parameters for the digital processing integrated circuit.

4. The on-chip real time clock module of Claim 1, wherein the digital processing integrated circuit is powered by an on-chip DC-to-DC converter.

5. The on-chip real time clock module of Claim 1, wherein the on-chip real time clock module remains active when the digital processing integrated circuit is powered down.

6. The on-chip real time clock module of Claim 3, wherein a processor within the digital processing integrated circuit directs the on-chip real time clock module to store the operational parameters and timing parameters of the digital processing integrated circuit in the persistent registers at a predetermined frequency.

7. The on-chip real time clock module of Claim 3, wherein a processor within the digital processing integrated circuit directs the on-chip real time clock module to supply the operational parameters and timing parameters from the persistent registers to the digital processing integrated circuit at startup.

8. The on-chip real time clock module of Claim 3, wherein the on-chip real time clock module interrupts the digital

processing integrated circuit when an alarm clock setting is reached.

9. The on-chip real time clock module of Claim 3, wherein:

the on-chip real time clock module directs the digital processing integrated circuit to power up when an alarm clock setting is reached; and

the on-chip real time clock module supplies the operational parameters and timing parameters of the digital processing integrated circuit in the persistent registers at power up.

10. The on-chip real time clock module of Claim 3, wherein a processor within the digital processing integrated circuit directs the on-chip real time clock module to supply the operational parameters and timing parameters of the digital processing integrated circuit in the persistent registers when the operational parameters and timing parameters of the digital processing integrated circuit are stale.

11. The on-chip real time clock module of Claim 3, wherein a processor within the digital processing integrated circuit directs the on-chip real time clock module to store the operational parameters and timing parameters of the digital processing integrated circuit in the persistent registers when the battery reserve drops below a predetermined threshold, and then directs the digital processing integrated circuit to power down.

12. The on-chip real time clock module of Claim 1, wherein the on-chip real time clock are located on an audio processing chip.

13. A digital processing integrated circuit that comprises:

a plurality of integrated circuits;

a system clock module operably coupled to produce a system clock from a crystal oscillator;

a DC-to-DC converter operably coupled to power the digital circuitry and the system clock module from a battery; and

an on-chip real time clock module that comprises:

a plurality of persistent registers to store operational parameters and timing parameters of the digital processing integrated circuit, wherein the plurality of persistent registers are power by a battery and receive a timing signal from a crystal oscillator;

a clock domain crossing module operably coupled to the plurality of persistent registers, wherein the clock crossing domain module synchronizes a crystal oscillator clock domain produced by the crystal oscillator and a system clock domain produced by a system clock circuit of the digital processing integrated circuit;

an input buffer operably coupled to receive operational parameters and timing parameters from the digital processing integrated circuit in accordance with the system clock domain and to provide the operational parameters and timing parameters to one of the plurality of persistent registers in accordance with the crystal oscillator clock domain; and

an output buffer operably coupled to retrieve operational parameters and timing parameters from the plurality of persistent registers in accordance with

the crystal clock domain and to provide the retrieved operational parameters and timing parameters to the digital processing integrated circuit in accordance with the system clock domain.

14. The digital processing integrated circuit of Claim 13 that further comprises an interface between the on-chip real time clock module and the digital processing integrated circuit.

15. The digital processing integrated circuit of Claim 13 that further comprises a controller operable to direct the on-chip real time clock module to store operational parameters and timing parameters from the digital processing integrated circuit or retrieve operational parameters and timing parameters for the digital processing integrated circuit.

16. The digital processing integrated circuit of Claim 13 wherein the digital processing integrated circuit is powered by an on-chip DC-to-DC converter.

17. The digital processing integrated circuit of Claim 13 wherein the on-chip real time clock module remains active when the digital processing integrated circuit is powered down.

18. The digital processing integrated circuit of Claim 17, wherein a processor within the digital processing integrated circuit directs the on-chip real time clock module to store the operational parameters and timing parameters of the digital processing integrated circuit in the persistent registers at a predetermined frequency.

19. The digital processing integrated circuit of Claim 17, wherein a processor within the digital processing integrated circuit directs the on-chip real time clock module to supply the operational parameters and timing parameters of the digital processing integrated circuit in the persistent registers at startup.

20. The digital processing integrated circuit of Claim 17, wherein the on-chip real time clock module may interrupt the digital processing integrated circuit when an alarm clock setting is reached.

21. The digital processing integrated circuit of Claim 17, wherein:

the on-chip real time clock module directs the digital processing integrated circuit to power up when an alarm clock setting is reached; and

the on-chip real time clock module supplies the operational parameters and timing parameters of the digital processing integrated circuit in the persistent registers at power up.

22. The digital processing integrated circuit of Claim 17, wherein a processor within the digital processing integrated circuit directs the on-chip real time clock module to supply the operational parameters and timing parameters of the digital processing integrated circuit in the persistent registers when the operational parameters and timing parameters of the digital processing integrated circuit are stale.

23. The digital processing integrated circuit of Claim 17, wherein a processor within the digital processing integrated circuit directs the on-chip real time clock module to store the

operational parameters and timing parameters of the digital processing integrated circuit in the persistent registers when the battery reserve drops below a predetermined threshold, and then directs the digital processing integrated circuit to power down.

24. A method of managing operational parameters and timing parameters of a digital processing integrated circuit located on an audio processing chip, that comprises:

periodically storing the operational parameters and timing parameters of a digital processing integrated circuit in an on-chip real time clock module for later use by a digital processing integrated circuit;

providing the on-chip real time clock module a power source that remains active when the digital processing integrated circuit is powered down;

providing the on-chip real time clock module a clock signal from a crystal oscillator that remains active when the digital processing integrated circuit is powered down; and

providing the operational parameters and timing parameters stored in the on-chip real time clock module to the digital processing integrated circuit when the operational parameters and timing parameters in the digital processing integrated circuit are stale.

25. The method of Claim 24, wherein the operational parameters and timing parameters stored in the digital processing integrated circuit are stored within shadow registers.

26. The method of Claim 25, wherein the operational parameters and timing parameters contained within the shadow registers return to a default condition when the digital processing integrated circuit is powered down.

27. The method of Claim 24, further comprising:

monitoring battery power levels to the audio processing chip;

directing the on-chip real time clock module to store current operational parameters and timing parameters from the digital processing integrated circuit; and

directing the digital processing integrated circuit to power down.

28. The method of Claim 24, wherein:

the on-chip real time clock module operates in a crystal oscillator clock domain; and

the digital processing integrated circuit operates in a system clock domain.

29. The method of Claim 28, that further comprises synchronizing the crystal oscillator clock domain and system clock domain with a clock domain-crossing module operably coupled to the plurality of persistent registers.

30. The method of Claim 24 further comprises:

buffering operational parameters and timing parameters from the digital processing integrated circuit in accordance with the system clock domain; and

buffering operational parameters and timing parameters from the on-chip real time clock module for the digital processing integrated circuit in accordance with the crystal clock domain.

31. The method of Claim 24, further comprises maintaining the on-chip real time clock module in a powered state the when the digital processing integrated circuit is powered down.

32. The method of Claim 24, wherein the operational parameters and timing parameters in the digital processing integrated circuit at startup is stale.

33. The method of Claim 24, further comprising issuing an interrupt from the on-chip real time clock module to the digital processing integrated circuit when an alarm clock setting is reached.

34. The method of Claim 33, wherein:

the on-chip real time clock module directs the digital processing integrated circuit to power up when an alarm clock setting is reached; and

the on-chip real time clock module supplies the operational parameters and timing parameters of the digital processing integrated circuit in the persistent registers at power up.